**DESIGN DOCUMENT- AXI4 PROJECT**

# CONTENTS

**CHAPTER 1 OVERVIEW**

1.1 Top level block diagram with interface signals ……………………………02

1.2 Description of Top-level interface signals…………………………………..02

**CHAPTER2 FIFO**

2.1 Functional description of Write FIFO………………………………………..05

2.2 Write FIFO interface signals.……..……………………………………….......05

2.3 Description of Write FIFO interface signals………………………………05

2.4 Functional description of Read FIFO…...……………………………………06

2.5 Read FIFO interface signals.……..………………………………………........06

2.6 Description of Read FIFO interface signals……………………………….06

**CHAPTER 3 DECODER**

3.1 Functional description of decoder ………………………………….……....07

3.2 Decoder Interface signals …………………………………........................08

3.3 Description of decoder interface signals ………………………………….09

**CHAPTER 4 AXI4 MASTER**

4.1 Functional description of AXI Master ……………………………………..11

4.2 AXI master interface signals ……………………………………………........11

4.3 Description of AXI master interface signals …………………………….11

**CHAPTER 5 SIMULATION RESULTS**………………………………………………………

**CHAPTER 6 SYNTHESIS RESULTS**…………………………………………………………

# CHAPTER 1 – OVERVIEW

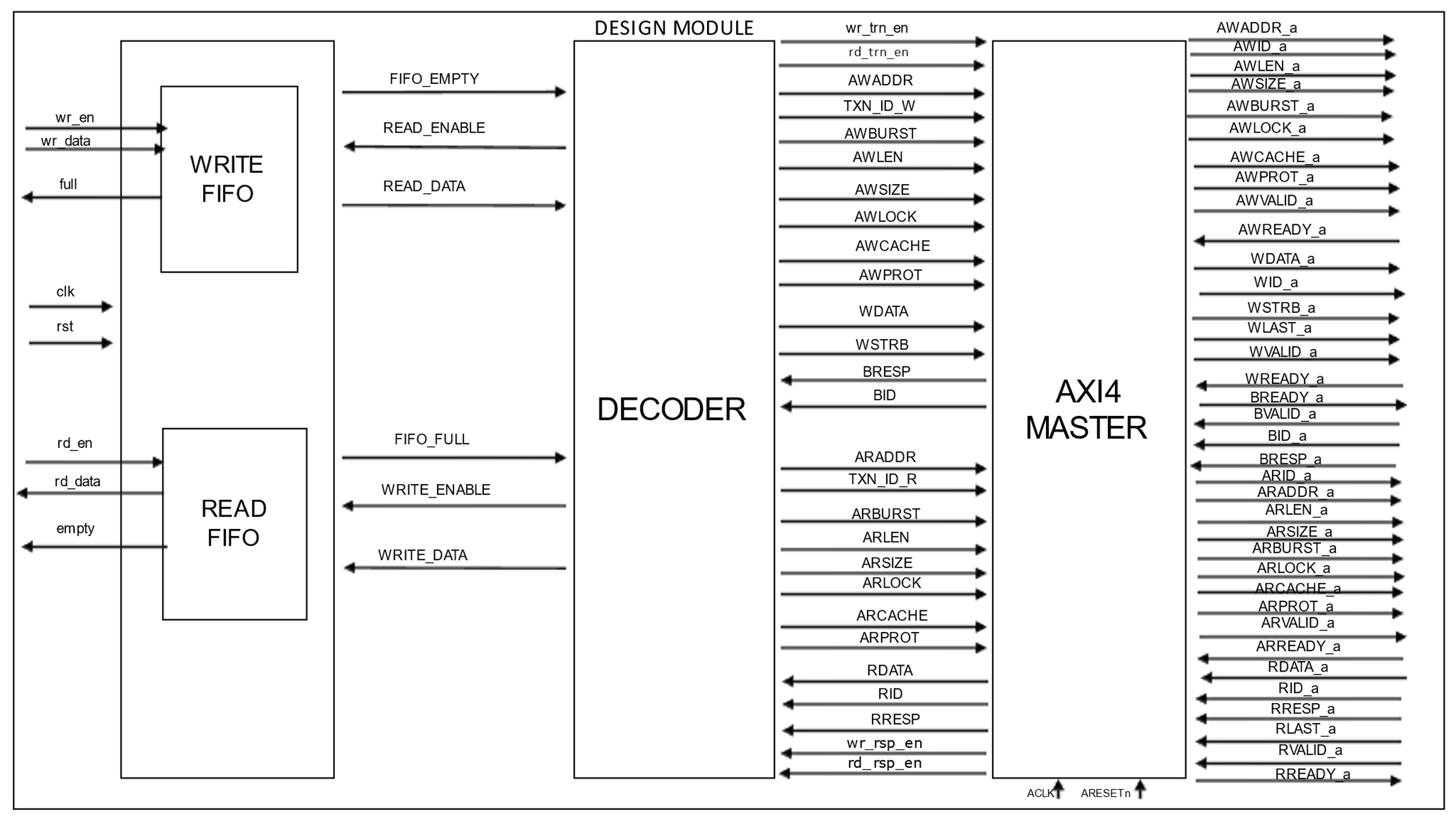
This design is a simple Packet Decoder with AXI4 master interface. The design consists of three blocks:

1. The FIFO interface consisting of read fifo and write fifo
2. The decoder
3. The AXI4 master interface

The CPU writes the packets into the write fifo. The decoder reads the packets from the write fifo and decodes the packets to extract address, control and data information. The decoded information is forwarded to the AXI4 master. The AXI4 master creates valid AXI4 write and read transactions from the decoded information.

The AXI4 master forwards the read data/response and write response to the decoder. The decoder forms the read data/response packet and write response packet and writes them into the read fifo. The CPU reads the response packets from the read fifo.

# Top-level block diagram with interface signals



* 1. **Description of Top-level interface signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal** | **SIZE (bits)** | **DIRECTION** | **Description** |
| clk | 1 | input | Global Clock signal with frequency of 100 Mhz. |
| rst | 1 | input | Global reset signal |
| wr\_en | 1 | input | Write enable. This signal is generated by the CPU. When high indicates that write fifo is enabled for writing the packet data. Write address/data phase packets and read address phase packets are written into the write fifo |
| rd\_en | 1 | input | Read Enable. This signal is generated by the CPU When high indicates that read fifo is enabled for reading the packet data. Write response packet and read data-response packets are read from the read fifo. |
| wr\_data | 128 | input | Write Data. This signal specifies the data to write into the write FIFO. |
| full | 1 | output | FIFO Full. This signal generated by write fifo, when asserted high indicates that write fifo is full, when asserted low indicates write fifo is not full |
| rd\_data | 128 | input | Read Data. This signal indicates the packet data read from the read fifo by the CPU |
| empty | 1 | output | FIFO Empty. This signal generated by read fifo, when asserted high indicates that read FIFO is empty, when asserted low indicates read fifo is not empty |
| ACLK | 1 | input | Global Clock Signal (100 MHz) |
| ARESETn | 1 | input | Global Reset Signal, active LOW |
| AWID\_a | 4 | output | Write Address ID. This signal is the identification tag for the write address group of signals |
| AWADDR\_a | 32 | output | Write Address. The write address gives the address of the first transfer in a write burst transaction |
| AWLEN\_a | 4 | output | Burst Length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address |
| AWSIZE\_a | 3 | output | Burst Size. This signal indicates the size of each transfer in the burst |
| AWBURST\_a | 2 | output | Burst Type. The burst type and the size information determine how the address for each transfer within the burst is calculated |
| AWLOCK\_a | 2 | output | Lock type. Provides additional information about the atomic characteristics of the transfer |
| AWCACHE\_a | 2 | output | Memory type. This signal indicates how transactions are required to progress through a system. |
| AWPROT\_a | 3 | output | Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. |
| AWVALID\_a | 1 | output | Write Address Valid. This signal indicates that the channel is signalling valid write address and control information |
| AWREADY\_a | 1 | input | Write Address Ready. This signal indicates that the slave is ready to accept an address and associated control signals |
| WID\_a | 4 | output | Write ID Tag. This signal is the ID tag of the write data transfer |
| WDATA\_a | 64 | output | Write Data. It can be of variable size depending on LEN and SIZE. Max size possible is 128 bytes = 1024 bits. |
| WSTRB\_a | 4 | output | Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus |
| WLAST\_a | 1 | output | Write Last. This signal indicates the last transfer in a write burst. |
| WVALID\_a | 1 | output | Write valid. This signal indicates that valid write data and strobes are available |
| WREADY\_a | 1 | input | Write Ready. This signal indicates that the slave can accept the write data |
| BID\_a | 4 | input | Response ID Tag. This signal is the ID tag of the write response. |
| BRESP\_a | 2 | input | Write Response. This signal indicates the status of the write transaction |
| BVALID\_a | 1 | input | Write Response Valid. This signal indicates that the channel is signalling a valid write response |
| BREADY\_a | 1 | output | Response Ready. This signal indicates that the master can accept a write response |
| ARID\_a | 4 | output | Read Address ID. This signal is the identification tag for the read address group of signals |
| ARADDR\_a | 32 | output | Read Address. The read address gives the address of the first transfer in a read burst transaction. |
| ARLEN\_a | 4 | output | Burst Length. This signal indicates the exact number transfers in a burst. |
| ARSIZE\_a | 3 | output | Burst Size. This signal indicates the size of each transfer in a burst. |
| ARBURST\_a | 2 | output | Burst Type. The burst type and the size information determine how the address of each transfer within the burst is calculated. |
| ARLOCK\_a | 2 | output | Lock type. This signal provides additional information about the atomic characteristics of the transfer |
| ARCACHE\_a | 2 | output | Memory type. This signal indicates how transactions are required to progress through a system |
| ARPROT\_a | 3 | output | Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. |
| ARVALID\_a | 1 | output | Read Address Valid. This signal indicates that the channel is indicating valid read address and control information. |
| ARREADY\_a | 1 | input | Read Address Ready. This signal indicates that the slave is ready to accept an address and associated control signals. |
| RID\_a | 4 | input | Read ID Tag. This signal is the identification tag for the read data group of signals generated by the slave. |
| RDATA\_a | 64 | input | Read data. It can be of variable size depending on LEN and SIZE. Max size possible is 128 bytes = 1024 bits. |
| RRESP\_a | 2 | input | Read Response. This signal indicates the status of the read transfer. |
| RLAST\_a | 1 | input | Read last. This signal indicates the last transfer the last transfer in a read burst. |
| RVALID\_a | 1 | input | Read valid. This signal indicates that the channel is signalling the required read data. |
| RREADY\_a | 1 | output | Read ready. This signal indicates that the master can accept the read data and response information. |

# Chapter 2 – FIFO

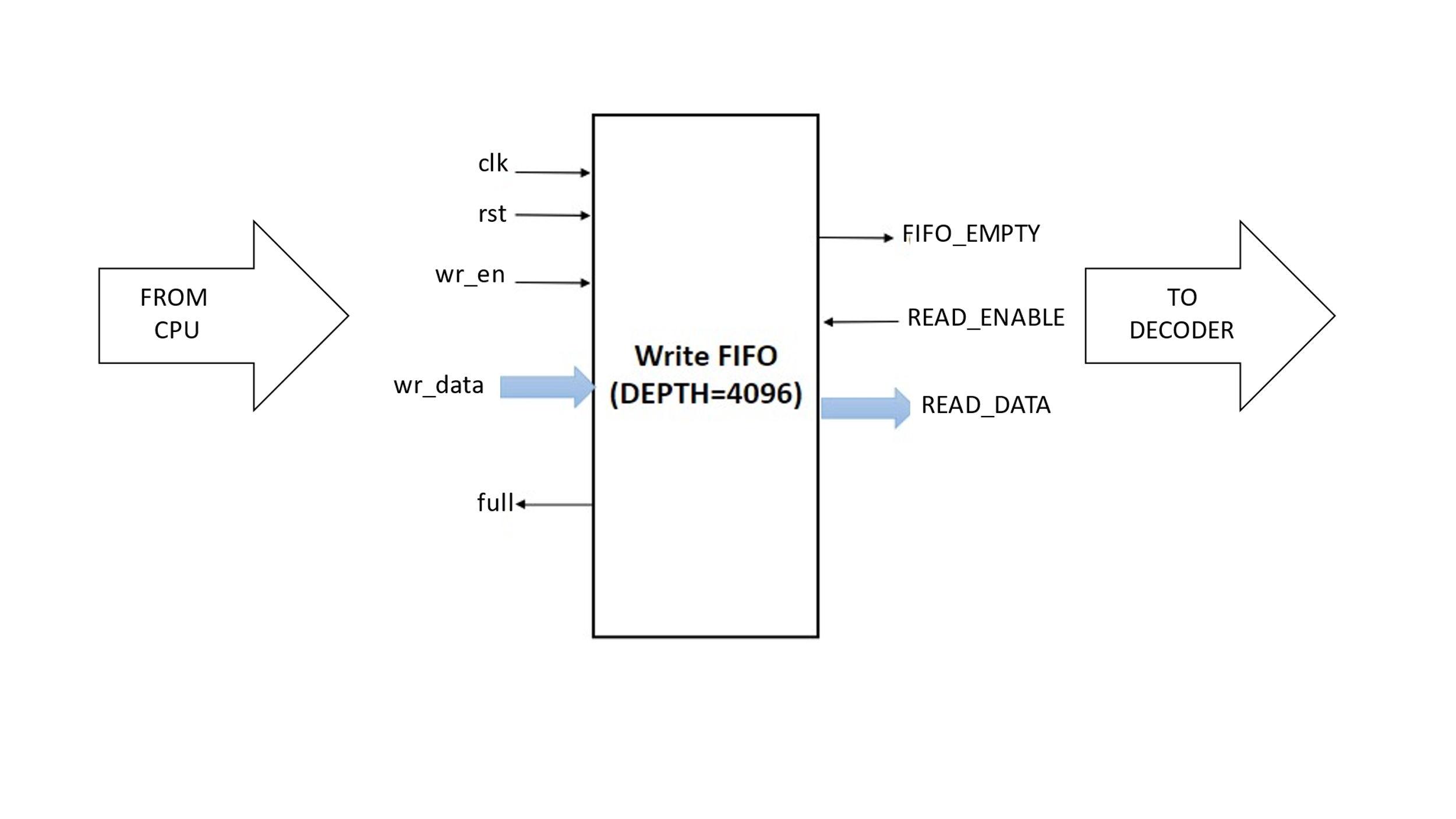
**2.1 Functional description of Write FIFO**

The CPU writes two types of packets into the write fifo:

1. Write data/address phase packets
2. Read address phase packets

The decoder reads the packets from the write fifo and decodes them. The write fifo is synchronous and 128 bits wide and 4096 deep.

**2.2 Write FIFO interface signals**



**2.3 Description of Write FIFO interface signals**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Signal name** | **Size in bits** | | **Direction** | | **Description** |
| Global signals | | | | | |
| clk | 1 | | input | | Global Clock signal with frequency of 100 Mhz. |
| rst | 1 | | input | | Global reset signal |
| Write FIFO | | | | | |
| wr\_en | 1 | | input | | Write enable. This signal enables to write the data into the write fifo. |
| READ\_ENABLE | 1 | | input | | Read Enable. This signal enables to read the data from the read fifo. |
| wr\_data | 128 | | input | | Write Data. This signal specifies the data to write into the FIFO. |
| FIFO\_EMPTY | | 1 | | output | FIFO Empty. This signal indicates the fifo empty condition. |
| full | | 1 | | output | FIFO Full. This signal indicates the fifo full condition. |
| READ\_DATA | | 128 | | output | Read data. This signal is used to read the data from the write fifo. |

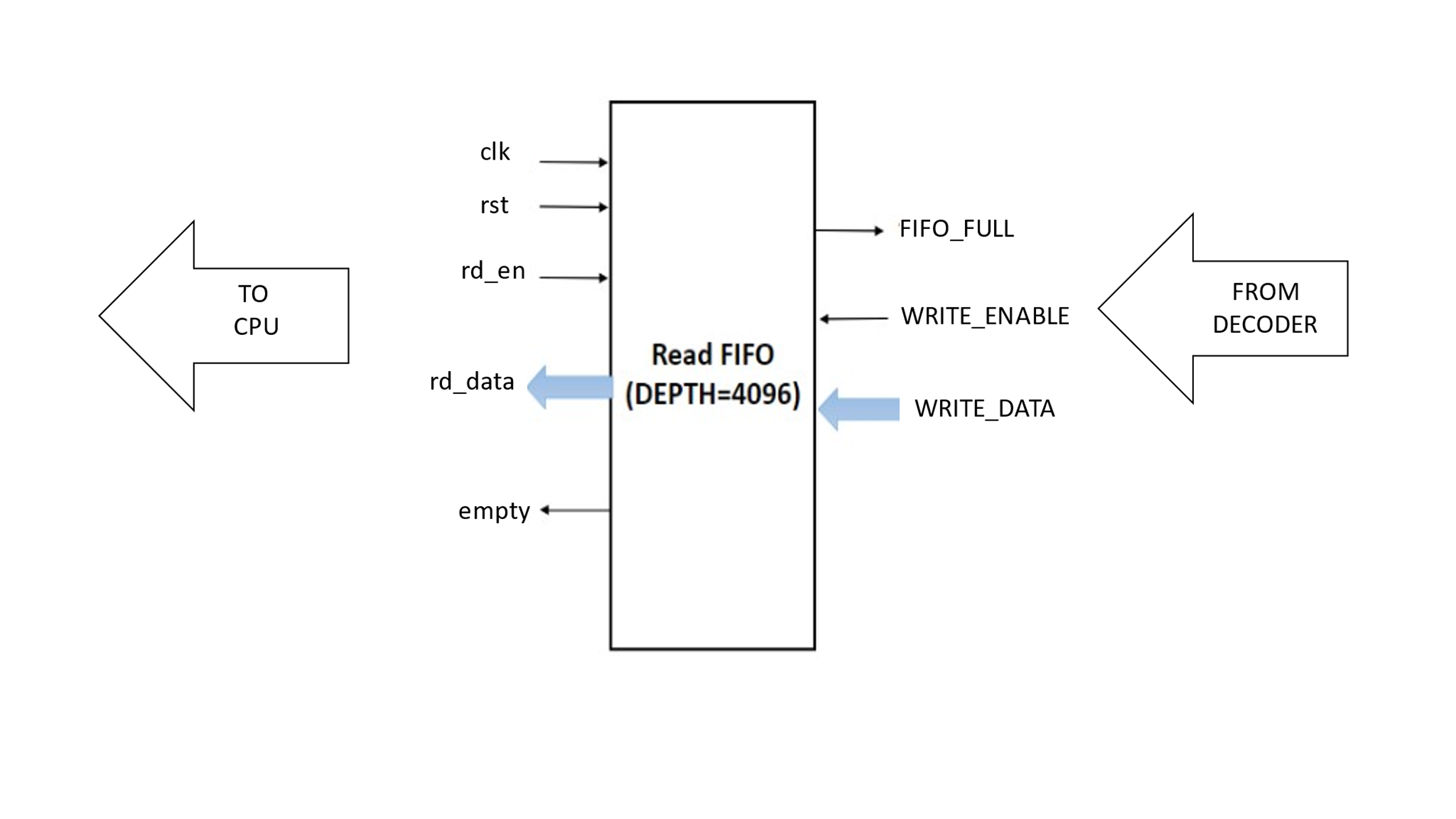
**2.4 Functional description of Read FIFO**

The decoder writes two types of packets into the read fifo:

1. Write response phase packets
2. Read data/response phase packets

The CPU reads the response packets from the read fifo. The read fifo is synchronous and 128 bits wide and 4096 deep.

**2.5 Read FIFO interface signals**



**2.6 Description of Read FIFO interface signals**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **Size in bits** | | **Direction** | **Description** |
| Global signals | | | | |
| clk | 1 | | input | Global Clock signal with frequency of 100 Mhz. |
| rst | 1 | | input | Global reset signal |
| Read FIFO | | | | |
| WRITE\_ENABLE | | 1 | input | Write enable. This signal enables to write the data into the read fifo. |
| rd\_en | | 1 | input | Read Enable. This signal enables to read the data from the read fifo. |
| WRITE\_DATA | | 128 | input | Write Data. This signal specifies the data to write into the fifo. |
| empty | | 1 | output | FIFO Empty. This signal indicates the fifo empty condition. |
| FIFO\_FULL | | 1 | output | FIFO Full. This signal indicates the fifo full condition. |
| rd\_data | | 128 | output | Read data. This signal specifies the data read from the fifo. |

# CHAPTER 3 – DECODER

## 3.1 **Functional description of decoder**

**Read Operation of The Decoder:** The decoder is going to decode the packet data from WRITE FIFO as follows.

Decoder checks for the FIFO\_EMPTY: -

* If FIFO\_EMPTY is High, then Decoder is not going to read any data from Write FIFO
* If FIFO\_EMPTY is Low, then Decoder asserts READ\_ENABLE and packet data is read from Write FIFO on read data lines.

The packet data stored in the Write FIFO can be any of the following types:

1. Write address/data phase packet

Packet = {SOP (8 bits) + TXN\_ID (4 bits) + ADDR (32 bits) + LEN (4 bits) + SIZE (3 bits) + BURST (2 bits) + LOCK (2 bits) + CACHE (2 bits) + PROT (3 bits) + STROBE (4 bits) + DATA (1024 bits) + EOP (8 bits)}

If the Data field >8bits and Data field! = 8’b00000000 then it is write address/data phase packet

1. Read address phase packet

Packet = {SOP (8 bits) + TXN\_ID (4 bits) + ADDR (32 bits) + LEN (4 bits) + SIZE (3 bits) + BURST (2 bits) + LOCK (2 bits) + CACHE (2 bits) + PROT (3 bits) + STROBE (4 bits) + DATA (8 bits) + EOP (8 bits)}

If the Data field =8bits and Data field = 8’b00000000 then it is Read Address phase packet

were

SOP= Start Of Packet =10101010

EOP= End Of Packet = 01010011

During Write Address phase/ Write Data phase/ Read Address phase, SOP and EOP fields are discarded. Based on the data field, the packet is identified as read packet or write packet. The packet is decoded to extract address, control and data information. The decoded data from the decoder is given to the AXI4 MASTER through user interface (AWADDR, AWID, AWBURST, AWLEN, AWSIZE, WDATA, WSTRB, WID, ARADDR, ARID, ARBURST, ARSIZE, ARLEN).

The packet data stored in the read FIFO can be any of the following types

1. Read Data/Response Phase Packet

Packet = {SOP(8 bits) + TXN\_ID(4 bits) + READ\_DATA(1024 bits) + READ\_RESP(4 bits) + EOP(8 bits)}

1. Write Response Phase Packet

Packet = {SOP(8 bits) + TXN\_ID(4 bits) + WRITE\_RESP(4 bits) + EOP(8 bits)}

where

SOP= Start Of Packet =10101010

EOP= End Of Packet = 01010011

The decoder module receives

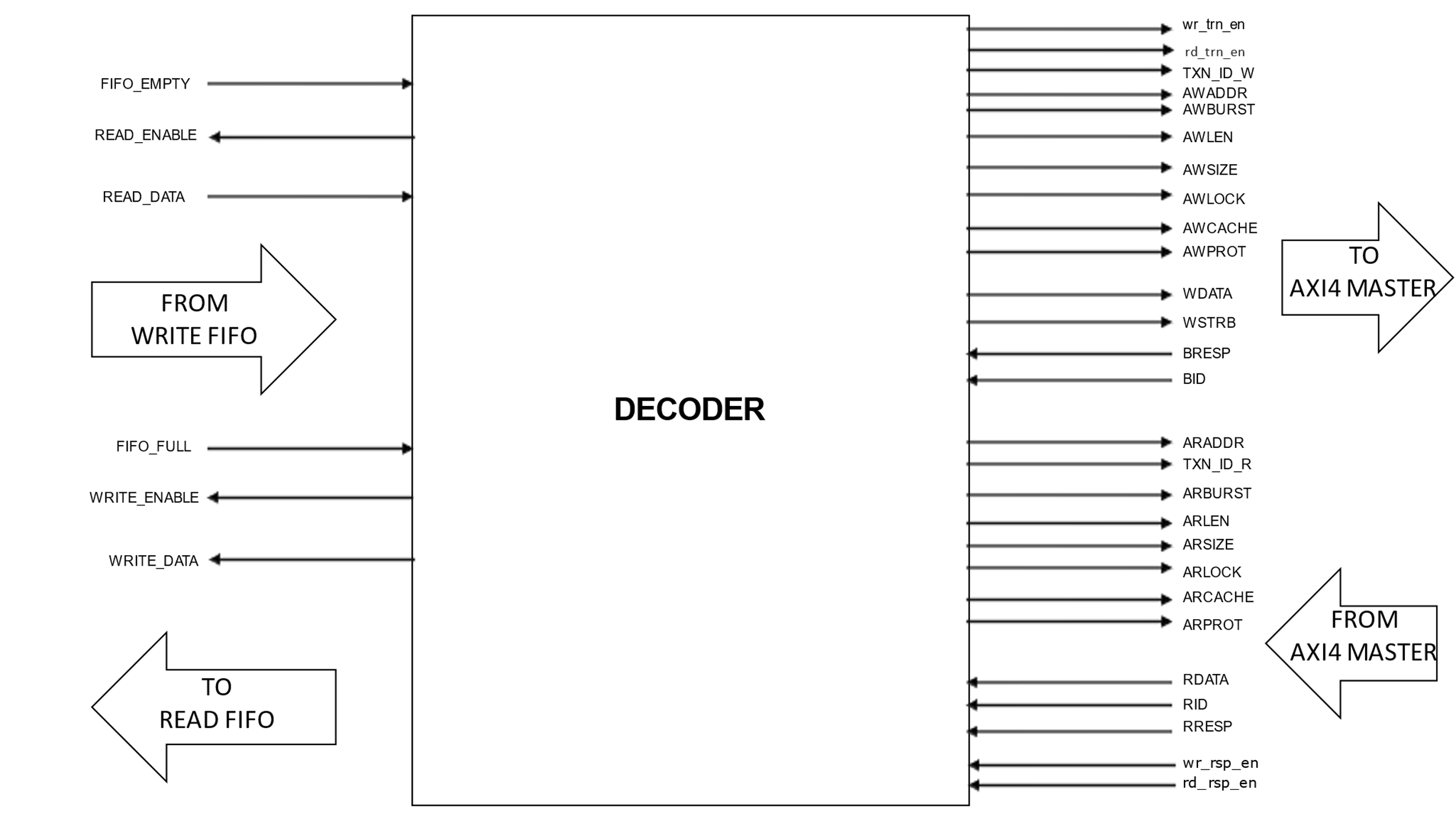
* Read data/response: For read data transaction, rd\_rsp\_en signal is asserted by AXI4 MASTER indicating valid read response followed by which AXI4 MASTER sends three signals to the Decoder that are RDATA, RID and RRESP. Decoder will create read data/response packet using these three signals as shown in the read data/response packet format above. This read data/response packet is then written into the READ\_FIFO.
* Write response: For Write data transaction, wr\_rsp\_en signal is asserted by AXI4 MASTER indicating valid read response followed by which AXI4 MASTER sends two signals to Decoder that are BRESP and BID. Decoder will create write response packet using these two signals as shown in the write response packet format. This write response packet is then written into the READ\_FIFO.

**Write Operation of The Decoder:** The decoder is going to write the packet data into the READ FIFO as follows

Decoder checks for the FIFO\_FULL before writing packet to the Read FIFO.

* If FIFO\_FULL is High, then Decoder is not going to write any data to the Read FIFO.
* If FIFO\_FULL is Low, then Decoder asserts WRITE\_ENABLE and WRITE\_DATA is written to the READ\_FIFO.

**3.2 Decoder Interface signals**



**3.3 Description of decoder interface signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal** | **SIZE (bits)** | **DIRECTION** | **Description** |
| AWADDR | 32 | OUTPUT | Write address after decoding the packet. The write address gives the address of the first transfer in a write burst transaction |
| TXN\_ID\_W | 04 | OUTPUT | Write address ID after decoding the packet. This signal is the identification tag for the write address group of signals |
| AWBURST | 02 | OUTPUT | Burst type after decoding the packet. The burst type and the size information, determine how the address for each transfer within the burst is calculated. |
| AWLEN | 04 | OUTPUT | Burst length after decoding the packet. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. |
| AWSIZE | 03 | OUTPUT | Burst size after decoding the packet. This signal indicates the size of each transfer in the burst. |
| AWLOCK | 02 | OUTPUT | Lock type after decoding the packet. Provides additional information about the atomic characteristics of the transfer |
| AWCACHE | 02 | OUTPUT | Memory type after decoding the packet. This signal indicates how transactions are required to progress through a system. |
| AWPROT | 03 | OUTPUT | Protection type after decoding the packet. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. |
| WDATA | 64 | OUTPUT | Write data after decoding the packet. It can be of variable size depending on LEN and SIZE. Max size possible is 128 bytes = 1024 bits. |
| WSTRB | 04 | OUTPUT | Write strobes after decoding the packet. This signal indicates which byte lanes hold valid data. There is one write strobe bit for every eight bits of the write data bus |
| BRESP | 02 | INPUT | Write response from AXI4 master. This signal indicates the status of the write transaction |
| BID | 04 | INPUT | Response ID tag from AXI4 master. This signal is the ID tag of the write response |
| ARADDR | 32 | OUTPUT | Read address after decoding the packet. The read address gives the address of the first transfer in a read burst transaction. |
| TXN\_ID\_R | 04 | OUTPUT | Read address ID after decoding the packet. This signal is the identification tag for the read address group of signals. |
| ARBUSRST | 02 | OUTPUT | Burst type after decoding the packet. The burst type and the size information determine how the address for each transfer within the burst is calculated. |
| ARSIZE | 03 | OUTPUT | Burst size after decoding the packet. This signal indicates the size of each transfer in the burst. |
| ARLEN | 04 | OUTPUT | Burst length after decoding the packet. This signal gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. |
| ARLOCK | 02 | OUTPUT | Lock type after decoding the packet. This signal provides additional information about the atomic characteristics of the transfer. |
| ARCACHE | 02 | OUTPUT | Memory type after decoding the packet. This signal indicates how transactions are required to progress through a system. |
| ARPROT | 03 | OUTPUT | Protection type after decoding the packet. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. |
| RDATA | 64 | INPUT | Read data from AXI4 master. It can be of variable size: 8,16,32,64,128,256,512,1024 bits wide; depending on ARLEN and ARSIZE. Max size possible is 128 bytes = 1024 bits. |
| RID | 04 | INPUT | Read ID tag from AXI4 master. This signal is the identification tag for the read data group of signals generated by the slave. |
| RRESP | 02 | INPUT | Read response from AXI4 master. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, DECSRR |
| RSTRB | 04 | OUTPUT | Read strobes. This signal is assumed to have a constant value of 4’b0000 for read packets |
| FIFO\_EMPTY | 1 | INPUT | This signal generated by write fifo, when asserted high indicates that write FIFO is empty, when asserted low indicates write FIFO is not empty. |
| READ\_ENABLE | 1 | OUTPUT | This signal is generated by the decoder. When high indicates that write FIFO is enabled for reading the packet data. Write Address data phase packets and Read Address phase packets are read from the write FIFO. |
| READ\_DATA | ~ 128 | INPUT | This signal indicates the packet data read from the write FIFO by the decoder. It can be 8,16,32,64,128,256,512,1024 bits wide. |
| FIFO\_FULL | 1 | INPUT | This signal generated by read FIFO, when asserted high indicates that read FIFO is full, when asserted low indicates read FIFO is not full |
| WRITE\_ENABLE | 1 | OUTPUT | This signal is generated by the decoder. When high indicates that read FIFO is enabled for writing the packet data. Write response packet and read data-response packets are written into read FIFO. |
| WRITE\_DATA | ~ 128 | OUTPUT | This signal indicates the packet data to write to the read FIFO by the decoder. It can be 8,16,32,64,128,256,512,1024 bits wide. |
| wr\_rsp\_en | 1 | INPUT | This is valid signal generated by AXI4 master in order to write response data. |
| rd\_rsp\_en | 1 | INPUT | This is valid signal generated by AXI4 master in order to read response data. |

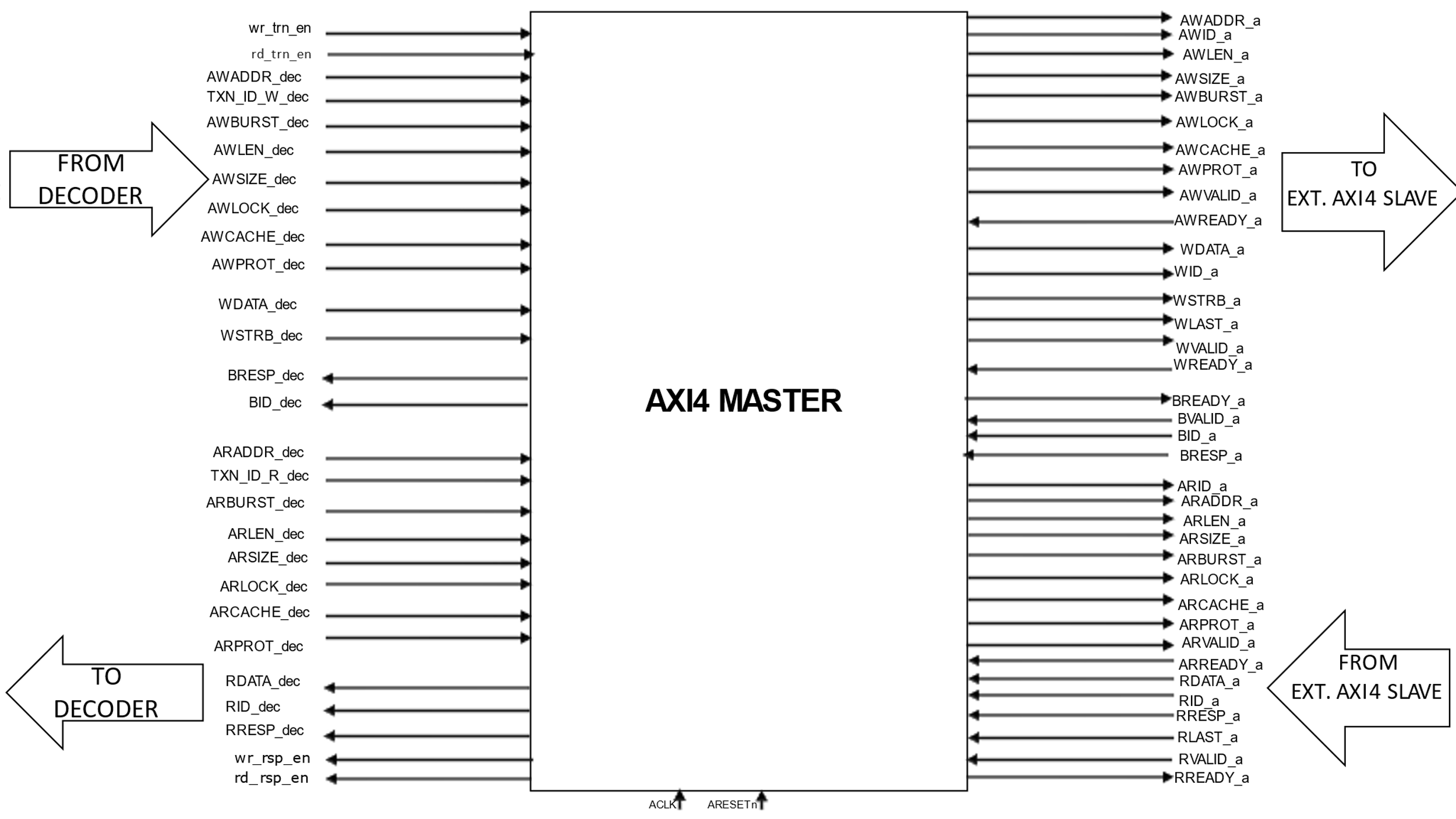
# CHAPTER 4 – AXI4 MASTER

**4.1 Functional description of AXI Master**

On the decoder side, the AXI4 master receives the decoded signals information and converts them into valid AXI4 write and read transactions. In order to take the proper response data, the response path from AXI master to Decoder should have valid signals, wr\_rsp\_en and rd\_rsp\_en.

On the external slave side, the AXI4 master receives read data/response and write response information and forwards it to the decoder

**4.2 Top Level block diagram with interface signals:**



**4.3 Description of AXI Slave Interface Signal:**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Size(bits) | Direction | Description |
| ACLK | 1 | IN | Global Clock Signal with frequency of 100 Mhz. |
| ARESETn | 1 | IN | Global Reset Signal, active LOW |
| AWID\_a | 4 | OUT | Write Address ID. This signal is the identification tag for the write address group of signals |
| AWADDR\_a | 32 | OUT | Write Address. The write address gives the address of the first transfer in a write burst transaction |
| AWLEN\_a | 4 | OUT | Burst Length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address |
| AWSIZE\_a | 3 | OUT | Burst Size. This signal indicates the size of each transfer in the burst |
| AWBURST\_a | 2 | OUT | Burst Type. The burst type and the size information determine how the address for each transfer within the burst is calculated |
| AWLOCK\_a | 2 | OUT | Lock type. Provides additional information about the atomic characteristics of the transfer |
| AWCACHE\_a | 2 | OUT | Memory type. This signal indicates how transactions are required to progress through a system. |
| AWPROT\_a | 3 | OUT | Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. |
| AWVALID\_a | 1 | OUT | Write Address Valid. This signal indicates that the channel is signalling valid write address and control information |
| AWREADY\_a | 1 | IN | Write Address Ready. This signal indicates that the slave is ready to accept an address and associated control signals |
| WID\_a | 4 | OUT | Write ID Tag. This signal is the ID tag of the write data transfer |
| WDATA\_a | 64 | OUT | Write Data. It can be of variable size depending on LEN and SIZE. Max size possible is 128 bytes = 1024 bits. |
| WSTRB\_a | 4 | OUT | Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus |
| WLAST\_a | 1 | OUT | Write Last. This signal indicates the last transfer in a write burst. |
| WVALID\_a | 1 | OUT | Write valid. This signal indicates that valid write data and strobes are available |
| WREADY\_a | 1 | IN | Write Ready. This signal indicates that the slave can accept the write data |
| BID\_a | 4 | IN | Response ID Tag. This signal is the ID tag of the write response. |
| BRESP\_a | 2 | IN | Write Response. This signal indicates the status of the write transaction |
| BVALID\_a | 1 | IN | Write Response Valid. This signal indicates that the channel is signalling a valid write response |
| BREADY\_a | 1 | OUT | Response Ready. This signal indicates that the master can accept a write response |
| ARID\_a | 4 | OUT | Read Address ID. This signal is the identification tag for the read address group of signals |
| ARADDR\_a | 32 | OUT | Read Address. The read address gives the address of the first transfer in a read burst transaction. |
| ARLEN\_a | 4 | OUT | Burst Length. This signal indicates the exact number transfers in a burst. |
| ARSIZE\_a | 3 | OUT | Burst Size. This signal indicates the size of each transfer in a burst. |
| ARBURST\_a | 2 | OUT | Burst Type. The burst type and the size information determine how the address of each transfer within the burst is calculated. |
| ARLOCK\_a | 2 | OUT | Lock type. This signal provides additional information about the atomic characteristics of the transfer |
| ARCACHE\_a | 2 | OUT | Memory type. This signal indicates how transactions are required to progress through a system |
| ARPROT\_a | 3 | OUT | Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. |
| ARVALID\_a | 1 | OUT | Read Address Valid. This signal indicates that the channel is indicating valid read address and control information. |
| ARREADY\_a | 1 | IN | Read Address Ready. This signal indicates that the slave is ready to accept an address and associated control signals. |
| RID\_a | 4 | IN | Read ID Tag. This signal is the identification tag for the read data group of signals generated by the slave. |
| RDATA\_a | 64 | IN | Read data. It can be of variable size depending on LEN and SIZE. Max size possible is 128 bytes = 1024 bits. |
| RRESP\_a | 2 | IN | Read Response. This signal indicates the status of the read transfer. |
| RLAST\_a | 1 | IN | Read last. This signal indicates the last transfer the last transfer in a read burst. |
| RVALID\_a | 1 | IN | Read valid. This signal indicates that the channel is signalling the required read data. |
| RREADY\_a | 1 | OUT | Read ready. This signal indicates that the master can accept the read data and response information. |
| wr\_rsp\_en | INPUT | 1 | This is valid signal generated by AXI4 master in order to write response data. |
| rd\_rsp\_en | INPUT | 1 | This is valid signal generated by AXI4 master in order to read response data. |